REMARKS

Entry of this Reply is respectfully requested because the Reply is considered to place the application in condition for allowance.

Claims 1 – 3, 5 and 15 – 32 are pending. Claims 15 – 29 have been withdrawn. Applicants respectfully request reconsideration and allowance of this application in view of the above amendments and the following remarks.

Claim 32 was rejected under 35 U.S.C. 112, second paragraph, as being indefinite. Particularly, the Examiner has asserted that it is not clear where a stratiform region is located, that it is not clear how the insulating layer is provided by the stratiform region, and that it is not clear if the insulating layer is the same or different to "a stratiform layer."

Claim 32 recites the novel embodiment in which the stratiform region forms the insulation layer in such a manner that the interstitial oxygen in the substrate is concentrated in a distortion layer at an interface between the epitaxial layer and the semiconductor substrate. As clearly disclosed on, for example, paragraph 31 of the publication of this application, the stratiform region (oxide film) 3 of SiO_2 is formed at the interface between the epitaxial layer 2 and the semiconductor substrate 1. Further, as clearly disclosed in the same paragraph, the stratiform region forms the insulating layer insulating layer 3, 34. Particularly, the stratiform region as the insulating layer 3 is disposed between the epitaxial layer 2 and the semiconductor substrate 1.

As also clearly disclosed on, for example, paragraph 40 of the publication of this application, oxygen in the high-resistance semiconductor substrate 31 that contains interstitial oxygen at a high concentration is deposited using as nuclei a distortion layer at the interface

between the epitaxial growth layer and the substrate so that a SiO_2 stratiform region 34 can be formed.

Therefore, because claim 32 recites clear and definite subject matter, namely that the stratiform region is located at the interface between the epitaxial layer and the semiconductor substrate, that the SiO_2 of the stratiform layer provides the insulating layer, and that the insulating layer is the same as the stratiform layer, it is respectfully requested that the rejection of claim 32 under 35 U.S.C. 112, second paragraph, be withdrawn.

Claims 1 – 2 and 30 – 31 were rejected under 35 USC 102(b) as being anticipated by U.S. Patent No. 5,611,855 to Wijaranakula. Applicants respectfully request that this rejection be withdrawn for the following reasons.

Claim 1 recites the novel embodiment disclosed, for example, on paragraphs 29 – 32 of a method for manufacturing a semiconductor substrate. The method comprises forming an epitaxial layer 2 on a semiconductor substrate 1 by epitaxial growth; and forming an insulating layer 3 by deposition at an interface between the epitaxial layer and the semiconductor substrate by performing a heat treatment that is performed in an oxidizing atmosphere. The heat treatment for forming the insulating layer is performed at a temperature higher than about 1100 Celsius.

Wijaranakula discloses a semiconductor silicon wafer 10 useful as a calibration standard for measurement of a thickness 18 of a microdefect-free layer 16 formed by depositing an epitaxial layer onto a substrate 12 having an interstitial oxygen concentration suitable for precipitating oxide. Large, uniform oxide microdefects 14 are formed in the substrate by maintaining the semiconductor silicon wafer at between 600 degrees Celsius and 900 degrees Celsius to nucleate oxide precipitates that are then grown at between 800 degrees Celsius and 1,200 degrees Celsius. Because the epitaxial layer contains no oxide precipitate nuclei to form

microdefects, the epitaxial layer remains a microdefect-free layer and has a relatively sharp, easily detectable boundary with the substrate.

Wijaranakula discloses microdefects 14 that are randomly disposed in the substrate 12 so that the transition region 30 is formed in the substrate 12. (See Col. 4, Lines 54 – 60). However, Wijaranakula fails to disclose forming an insulating layer by deposition at an interface between the epitaxial layer and the semiconductor substrate by performing a heat treatment that is performed in an oxidizing atmosphere.

The Examiner has asserted that the transition region 30 discloses an insulating layer. Applicants respectfully disagree. Particularly, the transition region 30 is composed of the silicon substrate 12 and the microdefects 14. The microdefects have a diameter in a range between 0.1 and 10 micrometers and a density greater than 10^9 defects/cm^3. (See Fig. 3). The transition region 30 does not disclose an insulating layer as recited in claim 1, as the transition region 30 is not disposed at the interface between the epitaxial layer 16 and the substrate 12. Rather, the transition region 30 is disposed in all of the substrate 12. Particularly, the oxide microdefects are distributed through the substrate 12. (See Col. 5, Line 50).

Therefore, because Wijaranakula fails to disclose forming an insulating layer by deposition at an interface between the epitaxial layer and the semiconductor substrate by performing a heat treatment that is performed in an oxidizing atmosphere, it is respectfully requested that the rejection of claim 1 under 35 U.S.C. 102(b) be withdrawn.

Claims 2 and 30 – 31 depend from claim 1. Therefore, the rejection of these claims should be withdrawn for at least the above-mentioned reasons with respect to claim 1.

Claims 3 and 32 were rejected under 35 U.S.C. 103(a) as being unpatentable over Wijaranakula. Applicants respectfully request that this rejection be withdrawn for the following reasons.

The Examiner has asserted that the claims range of concentration of Oxygen in the semiconductor substrate and the claimed range of thickness of the insulating layer are considered to be routine optimization. However, the recited limitations lead to unexpected results. A *prima facie* case of obviousness is rebutted by proof of unexpected or superior results. (See MPEP 2144.09 Aug. 2001). Particularly, as disclosed on, for example, paragraph 32, the method for manufacturing the semiconductor substrate for an SOI semiconductor device can dispense with many steps such as preparation of two mirror wafers for bonding, bonding of the two mirror wafers, heat treatment for bonding, edge treatment for obtaining a required SOI thickness, surface grinding, re-polishing for mirror finish, and several checks for voids, SOI thickness, and the like, in comparison with a conventional bonding method. In consequence, significant cost reduction can be achieved.

In summary, because the recited limitations lead to unexpected and superior results, it is respectfully requested that the rejection of claims 3 and 32 under 35 U.S.C. 103(a) be withdrawn.

Further, claims 3 and 32 depend from claim 1. Therefore, the rejection of claims 3 and 32 should be withdrawn for at least the above-mentioned reasons with respect to claim 1.

In view of the foregoing, Applicants submit that this application is in condition for allowance. A timely notice to that effect is respectfully requested. If questions relating to patentability remain, the examiner is invited to contact the undersigned by telephone.

If there are any problems with the payment of fees, please charge any underpayments and credit any overpayments to Deposit Account No. 50-1147.

Respectfully submitted,

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